WHAT IS CLAIMED IS:

1. A manufacturing method of a semiconductor device having a plurality of wiring layers, comprising the steps of:

forming a first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting said divided patterns, and exposing them, wherein a position of said connection is formed in parallel with a wiring which is formed by said first wiring layer; and

forming a second wiring layer, as a pattern, for forming a wiring having an area which intersects said connecting position by a batch processing of exposure.

2. A method according to claim 1, wherein the wiring which is formed by said first wiring layer does not have an area which overlaps said connecting position and the wiring which is formed by said second wiring layer has the area which overlaps said connecting position.

3. A method according to claim 1, wherein said first wiring layer is a horizontal direction wiring layer which is parallel with the connecting position for connecting said divided patterns and said second wiring layer is a vertical direction wiring layer

which perpendicularly crosses said connecting position.

4. A manufacturing method of a solid state image pickup device having pixels each having a photoelectric converting area for converting light into signal charges and a plurality of wiring layers including a first wiring layer and a second wiring layer, comprising the steps of:

forming the first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting said divided patterns, and exposing them, wherein a position of said connection is arranged in parallel with a wiring which is formed by said first wiring layer; and

forming the second wiring layer, as a pattern, for forming a wiring having an area which intersects said connecting position by a batch processing of exposure.

5. A method according to claim 4, wherein the wiring which is formed by said first wiring layer does not have an area which overlaps said connecting position for connecting said divided patterns and the wiring which is formed by said second wiring layer has the area which overlaps said connecting position.

6. A method according to claim 4, wherein a vertical direction wiring is formed by said first wiring layer and a horizontal direction wiring is formed by said second wiring layer.

7. A method according to claim 6, wherein said horizontal direction wiring is a drive wiring of said pixels.

8. A method according to claim 4, wherein before the step of forming said plurality of wiring layers, a CMOS process is included at the time of said pixel creation.

9. A method according to claim 1, wherein alignment of the pattern for forming said first wiring layer and the pattern for forming said second wiring layer is made by a die-by-die system.

10. A method according to claim 4, wherein alignment of the pattern for forming said first wiring layer and the pattern for forming said second wiring layer is made by a die-by-die system.

11. A semiconductor device having a plurality of wiring layers, wherein:

a wiring which is formed by a first wiring

layer is formed by divisional exposure, a connecting position at the time of said divisional exposure is formed in parallel with the wiring which is formed by said first wiring layer, and a wiring which is formed by a second wiring layer has an area which intersects said connecting position.